An American National Standard
Approved May 4, 2001

for the Electrostatic Discharge
Sensitivity Testing

Machine Model – Component Level
ESD Association Standard Test Method for Electrostatic Discharge Sensitivity Testing:

Machine Model-Component Level

Approved May 16, 1999
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Foreword

This test standard defines a method that simulates an ESD event occurring from a low resistance source. Component damage caused by the Machine Model (MM) is often similar to that caused by the Human Body Model (HBM), but occurs at a significantly lower voltage. Other forms of ESD-related component damage, such as that induced by the Charged Device Model (CDM), may result in a different failure signature for some components.

To fully characterize a component’s electrostatic discharge susceptibility, it should be tested to the following three ESD test standards:

- Human Body Model
- Charged Device Model
- Machine Model

Requirements for HBM and CDM testing are contained in the ESD Association Standards STM5.1 and DS5.3.1 respectively.

Users of this standard test method should understand that the data obtained when classifying components does not necessarily mean that the components will be unaffected if subjected to a lower level actual electrostatic discharge (ESD). This standard test method is intended to minimize test data correlation problems due to variations between testers.

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1. Scope and Purpose

1.1 Scope
This standard establishes the procedure for testing, evaluating, and classifying the electrostatic discharge (ESD) sensitivity of components to the defined machine model (MM).

1.1.1 Existing data
Data previously generated with testers meeting all waveform criteria of this standard shall be considered valid test data.

1.2 Purpose
The purpose of this standard is to establish a test method that will replicate MM failures and provide reliable, repeatable results from tester to tester, regardless of component type. Repeatable data will allow accurate comparisons of MM ESD sensitivity levels.

2. References

ESD-ADV1.0 Glossary of Terms
ESD - STM5.1 - Human Body Model (HBM)

3. Definitions

The following definitions are in addition to those in the EOS/ESD Glossary of Terms.

3.1 Component
An item such as a resistor, diode, transistor, integrated circuit or hybrid circuit.

3.2 Component failure
A condition in which a tested component does not meet one or more specified static or dynamic data sheet parameters.

3.3 Data sheet parameters
Static and/or dynamic component performance data supplied by the component manufacturer or user.

3.3.1 Static parameters are those measured with the component in a non-operating condition. These may include, but are not limited to: input leakage current, input breakdown voltage, output high and low voltages, output drive current, and supply current.

3.3.2 Dynamic parameters are those measured with the component in an operating condition. These may include, but are not limited to: full functionality, output rise and fall times under a specified load condition, and dynamic current consumption.

3.4 Electrostatic discharge sensitivity (ESDS)
The ESD level that causes component failure.

3.5 ESD withstand voltage
The maximum ESD level that does not cause component failure.

3.6 Human body model (HBM) electrostatic discharge (ESD)
An ESD event meeting the criteria specified in the Human Body Model standard test method STM5.1.

3.7 Machine model (MM) electrostatic discharge (ESD)
An ESD event meeting the criteria specified in this standard test method and based on a discharge network consisting of a charged 200 picofarad capacitor and (nominally) zero ohms of series resistance. Actual series resistance and inductance are specified in terms of the current waveform through a shorting wire. The simulation test approximates the electrostatic discharge from a machine.

3.8 MM ESD tester
Equipment (referred to as “tester” in this standard) that applies Machine Model ESD to a component.

3.9 Positive clamp socket
A positive clamp test socket is a zero insertion force (ZIF) socket with a clamping mechanism. It allows the shorting wire to be easily clamped.
into the socket. Examples are dual in-line package (DIP) and pin grid array (PGA) ZIF sockets.

3.10 Ringing
High frequency oscillation superimposed on the waveform.

3.11 Step stress test hardening
This occurs when a component subjected to increasing ESD voltage stresses is able to withstand higher stress levels than a similar component stressed at a single lower voltage level. For example: a component may fail at 100 volts if subjected to a single stress, but fail at 300 volts if stressed incrementally from 25 volts.

4. MM ESDS component classification
ESD sensitive components are classified according to their MM ESD withstand voltage, regardless of polarity. The MM ESDS component classification levels are shown in Table 1.

<table>
<thead>
<tr>
<th>Class</th>
<th>Voltage Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>&lt;100</td>
</tr>
<tr>
<td>M2</td>
<td>100 to &lt;200</td>
</tr>
<tr>
<td>M3</td>
<td>200 to &lt;400</td>
</tr>
<tr>
<td>M4</td>
<td>&gt; or = 400</td>
</tr>
</tbody>
</table>

5. Required equipment

5.1 MM ESD tester
An acceptable tester is composed of equipment meeting the requirements of this standard. (Schematically represented in Figure 1 and producing pulses meeting the waveform characteristics specified in Figures 2 and 3.)

5.2 Waveform verification equipment
Equipment capable of verifying the pulse waveforms defined in this standard includes, but is not limited to: an oscilloscope, two evaluation loads, and a current transducer.

5.2.1 Oscilloscope
Oscilloscope requirements:
- Minimum sensitivity of 100 milliampere per major division (typically one centimeter) when used in conjunction with the current transducer specified in section 5.2.3.
- Minimum single shot bandwidth of 350 megahertz.
- Minimum writing rate of one major division per nanosecond.

5.2.2 Evaluation loads
Two evaluation loads are necessary to verify tester functionality:
- Load 1: A solid 18 to 24 AWG (0.81 to 0.21 mm² cross section) tinned copper shorting wire not longer than 75 millimeters in length.
- Load 2: A 500 ohm, ± 1%, 1000 volt, low inductance, sputtered film resistor (Caddock Industries type MG 714 or equivalent).

Note 1: Due to an increased inductance value, wire-wound resistors are not acceptable for use as the 500 ohm evaluation load.

The lead length of both evaluation loads should be as short as possible. The wire should span the distance from the reference pin to any other pin on the test socket while passing through the current transducer.

5.2.3 Current transducer
Current transducer requirements:
- Minimum bandwidth of 350 megahertz.
- Peak pulse capability of 15 ampere.
- Rise time of less than 1 nanosecond.
- Capable of accepting a solid conductor of 1.5 millimeters in diameter.
- Provide an output voltage per milliampere as required in section 5.2.1.a. (Usually one to five millivolt per milliampere).

A Tektronix CT-1, CT-2, or equivalent with a maximum cable length of 1 meter meets these requirements. A CT-2 probe or equivalent should be used if testing above 800 volts.

6. Equipment, waveform and qualification requirements

6.1 Equipment calibration
Calibrate all equipment used to evaluate the tester periodically in accordance with the manufacturer’s recommendation. This includes the oscilloscope, current transducer and high voltage resistor load. Maximum time between calibrations is one year. Calibration shall be traceable to national standards, such as the National Institute of Standards and Technology.
(NIST) in the United States, or international standards.

6.2 Tester qualification and requalification
Perform tester qualification procedures as part of the acceptance testing when the ESD tester is delivered. Refer to the manufacturer’s recommendations for acceptance testing procedures.

Perform requalification in accordance with section 7.2 following repairs or servicing that could affect the waveform. The maximum time between full requalification tests shall be one year. Retain all waveform records for the life of the tester or for the duration specified by the internal record keeping procedures.

6.3 Test fixture board qualification
Perform the test fixture board qualification procedure in accordance with section 7.3 on all new test fixture boards and any existing boards not previously checked.

The waveform check is required for positive clamp sockets each time the test fixture board is changed. The waveform check is recommended for all other socket types. Refer to section 7.1 for procedures.

6.4 Verify the ESD tester functionality in accordance with section 7.4 at least once per shift. Longer periods between tester checks may be used if no changes in waveforms are observed for several consecutive checks. However, if the waveforms no longer meet the specified limits, all ESD stress tests subsequent to the previous satisfactory waveform check shall be considered invalid.

Note 2: If ESD stress testing is performed on consecutive shifts, tester checks at the end of one shift may also serve as the initial check for the following shift.

7. Qualification and verification procedures

7.1 Waveform capture procedure
Use the following procedure to verify the waveforms:

7.1.1 The reference pin pair is defined as the pin pair with the shortest and the longest path to the pulse generation circuit. This information is typically supplied by the board designer or manufacturer.

7.1.2 To capture a waveform using a shorting wire, connect the pin with the shortest wiring path to terminal B. Place the shorting wire through the current transducer, as close to terminal B as practical, observing the polarity shown in Figure 1. Connect the other end of the wire to the pin to be tested. This pin is referred to as terminal A.

Note 3: For non-positive clamp sockets, attach the shorting wire to the wiring of the test fixture board between the socket pins connected to terminals A and B. The connection points shall be as close as possible to the test socket pins.

7.1.3 To capture a waveform using the 500 ohm resistor, replace the shorting wire with the resistor. Refer to Figure 1 to determine placement of the resistor in relation to the current transducer.

7.2 Tester qualification and requalification procedure
Use the following procedure for qualification and requalification of the tester:

7.2.1 Test the high voltage discharge path and all associated circuitry (sometimes referred to as Self Test or VI Test) according to the equipment manufacturer’s procedures.

7.2.2 If the equipment has a test point capture location, capture a waveform from the high voltage pulse generator. Refer to the tester manufacturer manual for procedures. Verify the waveform is within 10% of the expected output.

7.2.3 Using the shorting wire and an applied voltage of 100, 200 and 400 volts, record positive and negative waveforms on the reference pin pair and any other pins recommended by the equipment manufacturer. Verify the waveforms meet the specification in Figure 2.

7.2.4 To test for spurious pulses, set the horizontal time scale of the oscilloscope to one millisecond per division. Using the shorting wire, initiate a pulse and verify that any spurious pulse is less than 15% of the amplitude of the main pulse.

7.2.5 Using the 500 ohm resistor and an
applied voltage of ±400 volts, record waveforms for the reference pin pair. Verify the waveforms meet the specification in Figure 3.

7.3 Test fixture board qualification procedure
Use the following procedure for qualification of test fixture boards:

7.3.1 Verify electrical continuity for all pins on the test fixture board.

7.3.2 Capture a waveform for the reference pin pair and any other pin combinations recommended by the manufacturer of each socket on the board using the shorting wire and a ±400 volt pulse. Verify the waveforms meet the specification in Figure 2.

7.3.3 Capture a waveform on the reference pin pair using the 500 ohm resistor. Use an applied voltage of ±400 volts. Verify the waveforms meet the specifications in Figure 3.

7.4 Daily tester functionality check procedure
Use the following procedure to verify tester functionality:

7.4.1 Test the high voltage discharge path and all associated circuitry at the beginning of each day during which ESD stress testing is performed. Use the tester manufacturer's recommended procedure. If any failure is detected, do not perform testing with the sockets that use the defective discharge paths. Repair the tester and then requalify it in accordance with section 7.2.

7.4.2 Verify the waveform integrity at least once per shift. If necessary, remove the test fixture board being used and replace with a positive clamp socket test fixture board to facilitate waveform measurements. Verify the waveform using the shorting wire at ±400 volts, or the stress level to be tested.

8. MM testing requirements
Perform ESD stress testing at room temperature in accordance with the procedure below. It is permissible to use any voltage level in Table 3 as the starting stress level. Additional stress levels to those in Table 3 may be used (e.g., the additional voltages in Table 1). Three new components may be used at each voltage level and/or pin combination if desired. This will eliminate any possible step stress hardening effects and reduce the possibility of early failure due to cumulative stress on power pins. If three new components are used at each voltage level, it is recommended not to skip any stress level; this will avoid missing possible ESD vulnerability windows. Classify components according to their MM ESD withstand voltage.

ESD classification testing shall be considered destructive to the component, even if no component failure occurs.

8.1 Component handling
Use ESD damage prevention procedures when handling components before, during and after testing.

8.2 Component static and dynamic tests
To determine whether components have failed, perform static and dynamic testing to all data sheet parameters before and after ESD testing. Pin leakage current may only be used as a guide in determining the component ESD withstand voltage. It is not sufficient, especially for complex integrated circuits, to use pin leakage as the only criterion for component failure.

8.3 Test temperature
Stabilize the component at room temperature prior to and during the ESD stress testing period.

8.4 Sample Size
A minimum of three components is required for each stress level of the test.

8.5 Pin combinations
The pin combinations to be used for ESD stressing of all integrated circuit components are given in Table 2. Pin combination (n) is the total number of pin combinations. This varies from component to component depending on the number of power pin groups with the same name.

Vps(i) in Table 2, is any set of like named power supply or ground pins (e.g., Vcc, Vss, Vdd, analog GND, digital GND, etc.) which are metallically connected (within 2 ohms) on the chip or within the package. Like named pins that are resistively connected via the chip substrate or wells, or are electrically isolated from each other (more than 2 ohms), are considered separate sets for the purpose of these tests. For example, if two pins are labeled Vcc, but are not metallically connected (within 2 ohms) on the
chip or within the package, they shall be treated as distinct and separate Vps(i) sets. Only those pins which supply current to or interface to other pins shall be considered to be power pins.

Pins such as Vcc, Vdd, GND, Vss, Vee, +Vs and -Vs are considered power supply pins. These pins supply current to input and output buffers in such a way as to interface closely with the environment through other pins.

Pins such as offset adjust, compensation, clocks, controls, address, data, Vref, no connects (NC), output and input pins are considered non-power supply pins. For example, a programming power pin, usually called Vpp, shall be considered to be a non-power supply pin because it does not supply current to or interface with any other pins, and is not a diode drop away from any non-power pins.

For further clarification on pin combinations, see example in Appendix A.

**8.5.1** Discrete components and component arrays (including both passive and active components) shall be tested using all possible pin pair combinations (one pin to terminal A, another pin to terminal B) regardless of pin name or function.

9. **MM ESD stress testing procedure**

Test a minimum of three samples of the component to all specified static and dynamic data sheet parameters.

9.1 Determine the starting stress voltage level from Table 3. Select the first pin combination to be tested as stated in section 8.5.

9.2 Apply three positive and three negative pulses to the component. The interval between pulses shall be at least 1 second. Repeat this process using all other pin combinations specified in section 8.5.

---

**Table 2 - Pin combinations for all digital, analog, and hybrid integrated circuit components**

<table>
<thead>
<tr>
<th>Pin Combination Set</th>
<th>Connect Individually to Terminal A (Stress)</th>
<th>Connect to Terminal B (Ground)</th>
<th>Floating Pins (unconnected)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>All pins one at a time, except the pin(s) connected to terminal B</td>
<td>Vps(1) [First power pin(s)]</td>
<td>All pins except pin under test (PUT) and Vps(1) [First power pin(s)]</td>
</tr>
<tr>
<td>2</td>
<td>All pins one at a time, except the pin(s) connected to terminal B</td>
<td>Vps(2) [Second power pin(s)]</td>
<td>All pins except PUT and Vps(2) [Second power pin(s)]</td>
</tr>
<tr>
<td>i</td>
<td>All pins one at a time, except the pin(s) connected to terminal B</td>
<td>Vps(i) [ith power pin(s)] [1,2, ...i]</td>
<td>All pins except PUT and Vps(i)</td>
</tr>
<tr>
<td>n-1</td>
<td>All pins one at a time, except the pin(s) connected to terminal B</td>
<td>Vps(n-1)</td>
<td>All pins except PUT and Vps(n-1)</td>
</tr>
<tr>
<td>n</td>
<td>All non-Vps(i) pins, one at a time</td>
<td>All other non-Vps(i) pins, except the pin connected to terminal A</td>
<td>All Vps(i) pins</td>
</tr>
</tbody>
</table>
### Table 3 - MM ESD stress levels

<table>
<thead>
<tr>
<th>Stress Level</th>
<th>Equivalent Charging (±) Voltage Vp (volt)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
</tr>
<tr>
<td>2</td>
<td>200</td>
</tr>
<tr>
<td>3</td>
<td>400</td>
</tr>
</tbody>
</table>

9.3 Test the components to full static and dynamic data sheet parameters and record the results for each component. Perform parametric and functional testing at room temperature. If testing is required at multiple temperatures, perform testing at the lowest temperature first.

9.4 If all three components pass the specified data sheet parameters, repeat sections 9.1 through 9.3 using the next higher stress level of Table 3.

9.5 If one or more components fail, repeat the ESD stress test using three new components starting at the next lower stress level. If the components continue to fail, decrease the stress voltage until level 1 is reached. If any additional failures are observed at level 1, stop all testing at this level.

### 10. Classification Criteria

10.1 Classify the component to the highest passing MM ESD stress voltage level from Table 1 at which all three components pass full static and dynamic data sheet parameters following ESD testing.
Figure 1: Typical equivalent MM ESD stress test circuit

The performance of the tester is strongly influenced by parasitic capacitance and inductance.

Requirements:

1. The 500 ohm ±1% resistor R2 and shorting wire are specified in section 5.2.2.
2. The current transducer is specified in section 5.2.3.
3. Reversal of terminals A and B to achieve dual polarity performance is not permitted.
4. SW1 is closed 10 to 100 milliseconds after the pulse delivery period to ensure the socket is not left in a charged state. It should be opened at least 10 milliseconds prior to the delivery of the next pulse. The resistance R1 in series with the switch ensures a slow discharge of the device, thus avoiding the possibility of a charged device model discharge.
5. The Dual Polarity Pulse Generator shall be designed to avoid recharge transients and double pulses.
6. Piggybacking of test sockets (the insertion of secondary sockets into the main test socket) is allowed only if the secondary socket waveform meets the requirements of this standard.
Figure 2: Current waveform through a shorting wire for a 400 volt discharge

Requirements:

The current pulse through a short circuit shall meet the following characteristics:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>socket pin count = 1 to 40 pins</td>
<td>socket pin count = 41 to 128 pins</td>
</tr>
<tr>
<td>Ip1 for 100 volt stress (ampere)</td>
<td>1.75 ±10%</td>
</tr>
<tr>
<td>Ip1 for 200 volt stress (ampere)</td>
<td>3.5 ±10%</td>
</tr>
<tr>
<td>Ip1 for 400 volt stress (ampere)</td>
<td>7.0 ±10%</td>
</tr>
<tr>
<td>Ip2 as % of Ip1, for all stress levels</td>
<td>67% to 90%</td>
</tr>
<tr>
<td>tpm (nanoseconds) (see Note 4)</td>
<td>66 to 90</td>
</tr>
</tbody>
</table>

Note 4: tpm is the period of the major pulse measured between the first zero crossing point, t1, and the third zero crossing point, t3.

Note 5: For larger pin count devices, the 20% tolerance may cause miscorrelation between testers; particularly if stress steps smaller than those specified in Table 2 are used.
Figure 3: Current waveform through a 500 ohm resistor for a 400 volt discharge

Requirements:

The current pulse through a 500 ohm resistor shall meet the following characteristics for a ± 400 volt discharge:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{PR}$ (ampere)</td>
<td>0.85 - 1.2</td>
</tr>
<tr>
<td>$I_{100}$ (ampere)</td>
<td>0.26 - 0.32</td>
</tr>
<tr>
<td>$I_{200}$ as % of measured $I_{100}$</td>
<td>35% to 45%</td>
</tr>
</tbody>
</table>
Appendix A: Example of pin combinations using Table 2.

The following example is intended to clarify the pin combinations given in Table 2. The example is for a 10 pin device with 2-Vdd, 2-Vss, 2-Vcc, 2-input and 2-output pins. It is assumed that the like-named power supply pins are metallically connected (within 2 ohms) on the chip or within the package. If not, each should be treated as an individual power supply pin. Power supply and ground pins include Vdd, Vcc, Vss, Gnd, +Vs, -Vs, etc. as defined in section 8.5. Pins such as offset adjust, compensation, clock, control, address, data, Vref, no connect, input and output shall be considered non-power supply pins. For each pin combination sequence, follow the procedure established in section 9. The sequence # in the table below refers to the order of pin combinations for stressing.

<table>
<thead>
<tr>
<th>Sequence number</th>
<th>Pin combination set</th>
<th>Connect to terminal A (stress)</th>
<th>Connect to terminal B (ground)</th>
<th>Float Pins (unconnected)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1st input pin</td>
<td>2-Vdd</td>
<td>all other 7 pins</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>2nd input pin</td>
<td>2-Vdd</td>
<td>all other 7 pins</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1st output pin</td>
<td>2-Vdd</td>
<td>all other 7 pins</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>2nd output pin</td>
<td>2-Vdd</td>
<td>all other 7 pins</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>1st Vcc pin</td>
<td>2-Vdd</td>
<td>all other 7 pins</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>2nd Vcc pin</td>
<td>2-Vdd</td>
<td>all other 7 pins</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1st Vss pin</td>
<td>2-Vdd</td>
<td>all other 7 pins</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>2nd Vss pin</td>
<td>2-Vdd</td>
<td>all other 7 pins</td>
</tr>
<tr>
<td>9</td>
<td>2</td>
<td>Repeat sequence 1 to 8, but swap Vdd and Vss</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>3</td>
<td>Repeat sequence 1 to 8, but swap Vdd and Vcc</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>4</td>
<td>1st input pin</td>
<td>output 1,2 and input 2</td>
<td>all Vdd, Vss and Vcc pins</td>
</tr>
<tr>
<td>12</td>
<td>4</td>
<td>2nd input pin</td>
<td>output 1,2 and input 1</td>
<td>all Vdd, Vss and Vcc pins</td>
</tr>
<tr>
<td>13</td>
<td>4</td>
<td>1st output pin</td>
<td>input 1,2 and output 2</td>
<td>all Vdd, Vss and Vcc pins</td>
</tr>
<tr>
<td>14</td>
<td>4</td>
<td>2nd output pin</td>
<td>input 1,2 and output 1</td>
<td>all Vdd, Vss and Vcc pins</td>
</tr>
</tbody>
</table>
Appendix B: MM STM5.2 Procedure Flow

Procedure

Is Equipment Qualified?
N -> Qualification & Verification Procedure Section 7.
Y -> Record Waveforms

Has Equipment been serviced?
Y -> Qualification & Verification Procedure Section 7.
N ->

New Shift? or Fixture board changed?
Y -> Waveform Capture Procedure Section 7.1
N ->

Daily Tester Diagnostics needed?
Y -> Daily Tester Functionality Check Section 7.4
N ->

Component Pre-ESD test Section 8.2
ESD Stress Procedure Section 9.
Component Post-ESD test Section 8.2
Component Classification Section 4. And 10.